Department of Higher Education
University of Computer Studies, Yangon
Fourth Year (B.C.Tech.)
Final Examination
Computer Architecture II (CT- 404)
September, 2018

Answer All Questions. **Time Allowed: 3 Hours**

1(a) Consider a register *R* which can be loaded from any of four independent sources under the control of the four separate signals c_0, c_1, c_2 and c_3. Illustrating control field patterns, show how *R* can be loaded from a specified source or no-operation condition in (i) unencoded for any *n* independent control signals. (8 marks)

(b) (i)Describe the reasons for using nanoprogramming in designing control store organization.(ii) The following parameters are cited for the 68000 design : storage of 650 microinstructions each with a format consisting of 70 control bits. If only 40 percent of these microinstructions are to be stored in nano-control memory, determine the saving of storage space for this two-level control memory model over one-level model. (8 marks)

2(a) Pipeline reservation table for 2-element vector summation is given in Figure 1 (i) initializing new instructions, demonstrate space-time diagrams in two different ways till clock cycle 17. (ii) Determine the average latency for each scheduling strategy. (iii) State which strategy achieves better efficiency and explain why? (10 marks)

	Time *t*								
Stage	1	2	3	4	5	6	7	8	9
S_1	x	x				x			
S_2		x	x				x		
S_3			x	x				x	
S_4				x	x				x

Figure 1. Pipeline reservation table for a four-stage pipeline

(b) (i) Define different types of data hazards that can occur in pipeline.

(ii) Write down the necessary conditions to be checked for detecting the data dependency hazards in (i). (8 marks)

3(a) (i) illustrate how 256K x 8 bit RAM can be constructed from 64 x 8 bit RAM in one-dimensional array. (ii) How many address bits are needed for this design? In the design illustration, provide how all the address and control lines are arranged. (8 marks)

(b) A magnetic hard-disk memory unit has average seek time of 7.9 ms with disk-rotation speed of 7200 rev/min. If the number of 512 bytes sectors per track ranges from 108 to 180, what would be (i) the average storage capacity per track (ii) average block access time per track and (iii) the data transfer rate? (8 marks)

4(a) Describe how nonpreemptive allocation processes. Using the appropriate illustrations, explain how first fit and best fit nonpreemptive allocation differ. (8marks)

(b) A computer has two-level virtual-memory system. The main memory M_1 and the secondary memory M_2 have average access time of 10^{-6} and 10^{-3} s, respectively. We know that the average access time for the memory hierarchy is 10^{-4} s, which is considered unacceptably high. Describe two ways in which memory access time could be reduced from 10^{-4} to 10^{-5}s. (8 marks)

5(a) In a paging system, memory M_1 has a capacity of *three* pages. The execution of a program requires reference to five distinct pages P_i, where i=1, 2, 3, 3, 4, 5 and i is the page address. The page address stream formed by executing the program is,

1 2 3 4 1 2 5 1 2 3 4 5

which means that the first page referenced is P_1, the second is P_2, and so on. (i) Illustrate the assignment of pages to M_1 using Least Recently Used. (ii) Repeat the case in (i) for M_1 having a capacity of *four* pages. (iii) From this replacement with two different memory capacities, what observation you have made? (10 marks)

(b) How caches are distinguished upon the types of information store? Discuss the advantages and disadvantages these designs. (6 marks)

6(a) Illustrate the interconnection structure of (i) linear, (ii) ring, (iii) star and compare them in terms of number of edges. (8 marks)

[**OR**]

Give a brief account on ***any one*** of the following;

(i) tristate logic circuits in the design of shared bus
(ii) vector interrupt

(b) With the necessary illustration, analyze polling bus-arbitration and independent requesting methods with respect to bus priority and number of bus request and bus grant lines. (10 marks)

[**OR**]

Briefly compare and contrast ***any two pairs*** given below:

(i) intrasystem communication and intersystem communication
(ii) synchronous data transfer with and without wait states
(iii) processor-level parallelism and instruction-level parallelism

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